





















































































































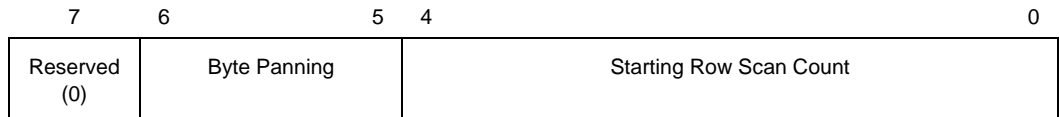


Bit De	scription
5	<p><b>Vertical Total Bit 9.</b> The vertical total is a 10-bit value that specifies the total number of scan lines. This includes the scan lines both inside and outside of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Total Register (CR06), and the most and second-most significant bits are supplied by this bit and bit 0, respectively, of this register.</p> <p>This 10-bit value should be programmed equal to the total number of scan lines, minus 2.</p>
4	<p><b>Line Compare Bit 8.</b> This bit provides the second most significant bit of a 10-bit value that specifies the scan line at which the memory address counter restarts at the value of 0. Bit 6 of the Maximum Scan Line Register (CR09) supplies the most significant bit, and bits 7-0 of the Line Compare Register (CR18) supply the 8 least significant bits. Normally, this 10-bit value is set to specify a scan line after the last scan line of the active display area. When this 10-bit value is set to specify a scan line within the active display area, it causes that scan line and all subsequent scan lines in the active display area to display video data starting at the very first byte of the frame buffer. The result is what appears to be a screen split into a top and bottom part, with the image in the top part being repeated in the bottom part. When used in cooperation with the Start Address High Register (CR0C) and the Start Address Low Register (CR0D), it is possible to create a split display, as described earlier, but with the top and bottom parts displaying different data. The top part will display what data exists in the frame buffer starting at the address specified in the two aforementioned start address registers, while the bottom part will display what data exists in the frame buffer starting at the first byte of the frame buffer.</p>
3	<p><b>Vertical Blanking Start Bit 8.</b> The vertical blanking start is a 10-bit that specifies the beginning of the vertical blanking period relative to the beginning of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Blanking Start Register (CR15), and the most and second-most significant bits are supplied by bit 5 of the Maximum Scan Line Register (CR09) and this bit of this register, respectively.</p> <p>This 10-bit value should be programmed to be equal to the number of scan lines from the beginning of the active display area to the beginning of the blanking period. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which the vertical blanking period begins.</p>
2	<p><b>Vertical Sync Start Bit 8.</b> The vertical sync start is a 10-bit value that specifies the beginning of the vertical sync pulse relative to the beginning of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Sync Start Register (CR10), and the most and second-most significant bits are supplied by bit 7 and this bit, respectively, of this register.</p> <p>This 10-bit value should be programmed to be equal to the number of scan lines from the beginning of the active display area to the start of the vertical sync pulse. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which the vertical sync pulse begins.</p>
1	<p><b>Vertical Display Enable End Bit 8.</b> The vertical display enable end is a 10-bit value that specifies the number of the last scan line within the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Display Enable End Register (CR12), and the two most significant bits are supplied by bit 6 and this bit, respectively, of this register.</p> <p>This 10-bit or value should be programmed to be equal to the number of the last scan line within in the active display area. Since the active display area always starts on the 0th scan line, this number should be equal to the total number of scan lines within the active display area, minus 1.</p>
0	<p><b>Vertical Total Bit 8.</b> The vertical total is a 10-bit value that specifies the total number of scan lines. This includes the scan lines both inside and outside of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Total Register (CR06), and the most and second-most significant bits are supplied by bit 5 and this bit, respectively, of this register.</p> <p>This 10-bit value should be programmed to be equal to the total number of scan lines, minus 2.</p>



## 2.6.10 CR08 —Preset Row Scan Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=08h)  
 Default: 0UUU UUUUb (U=Undefined)  
 Attributes: Read/Write



Bit De	scription															
7	<b>Reserved.</b> Read as 0s.															
6:5	<p><b>Byte Panning.</b> This field holds a 2-bit value that selects number of bytes (up to 3) by which the image is shifted horizontally to the left on the screen. This function is available in both text and graphics modes.</p> <p>In text modes with a 9-pixel wide character box, the image can be shifted up to 27 pixels to the left, in increments of 9 pixels. In text modes with an 8-pixel wide character box, and in all standard VGA graphics modes, the image can be shifted up to 24 pixels to the left, in increments of 8 pixels. When the Nine dot disable bit of the VGA control register is set, the pixel shift will be equivalent to the 8-dot mode.</p> <p>The image can be shifted still further, in increments of individual pixels, through the use of bits [3:0] of the Horizontal Pixel Panning Register (AR13).</p> <p style="text-align: center;"><b>Number of Pixels Shifted</b></p> <table style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">Bit [6:5]</th> <th style="text-align: left;">9-Pixel Text</th> <th style="text-align: left;">8-Pixel Text &amp; Graphics</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>0</td> <td>0</td> </tr> <tr> <td>01</td> <td>9</td> <td>8</td> </tr> <tr> <td>10</td> <td>18</td> <td>16</td> </tr> <tr> <td>11</td> <td>27</td> <td>24</td> </tr> </tbody> </table>	Bit [6:5]	9-Pixel Text	8-Pixel Text & Graphics	00	0	0	01	9	8	10	18	16	11	27	24
Bit [6:5]	9-Pixel Text	8-Pixel Text & Graphics														
00	0	0														
01	9	8														
10	18	16														
11	27	24														
4:0	<p><b>Starting Row Scan Count.</b> This field specifies which horizontal line of pixels within the character boxes of the characters used on the top-most row of text on the display will be used as the top-most scan line. The horizontal lines of pixels of a character box are numbered from top to bottom, with the top-most line of pixels being number 0. If a horizontal line of these character boxes other than the top-most line is specified, then the horizontal lines of the character box above the specified line of the character box will not be displayed as part of the top-most row of text characters on the display. Normally, the value specified by these 5 bits should be 0, so that all of the horizontal lines of pixels within these character boxes will be displayed in the top-most row of text, ensuring that the characters in the top-most row of text do not look as though they have been cut off at the top.</p>															



## 2.6.11 CR09 —Maximum Scan Line Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=09h)

Default: 00h

Attributes: Read/Write

7	6	5	4	0
Double Scanning	Line Cmp <9>	Vert Blank Start <9>	Starting Row Scan Count	

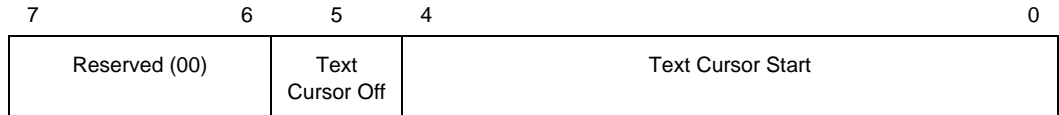
Bit De	scription
7	<p><b>Double Scanning Enable.</b></p> <p>0 = Disable. When disabled, the clock to the row scan counter is equal to the horizontal scan rate. This is the normal setting for many of the standard VGA modes.</p> <p>1 = Enable. When enabled, the clock to the row scan counter is divided by 2. This is normally used to allow CGA-compatible modes that have only 200 scan lines of active video data to be displayed as 400 scan lines (each scan line is displayed twice).</p>
6	<p><b>Line Compare Bit 9.</b> This bit provides the most significant bit of a 10-bit value that specifies the scan line at which the memory address counter restarts at the value of 0. Bit 4 of the Overflow Register (CR07) supplies the second most significant bit, and bits 7-0 of the Line Compare Register (CR18) supply the 8 least significant bits.</p> <p>Normally, this 10-bit value is set to specify a scan line after the last scan line of the active display area. When this 10-bit value is set to specify a scan line within the active display area, it causes that scan line and all subsequent scan lines in the active display area to display video data starting at the very first byte of the frame buffer. The result is what appears to be a screen split into a top and bottom part, with the image in the top part being repeated in the bottom part.</p> <p>When used in cooperation with the Start Address High Register (CR0C) and the Start Address Low Register (CR0D), it is possible to create a split display, as described earlier, but with the top and bottom parts displaying different data. The top part will display whatever data exists in the frame buffer starting at the address specified in the two aforementioned start address registers, while the bottom part will display whatever data exists in the frame buffer starting at the first byte of the frame buffer.</p>
5	<p><b>Vertical Blanking Start Bit 9.</b> The vertical blanking start is a 10-bit value that specifies the beginning of the vertical blanking period relative to the beginning of the active display area. The 8 least significant bits of this value are supplied by bits [7:0] of the Vertical Blanking Start Register (CR15), and the most and second-most significant bits are supplied by this bit and bit 3 of the Overflow Register (CR07), respectively.</p> <p>This 10-bit value should be programmed to be equal to the number of scan line from the beginning of the active display area to the beginning of the blanking period. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which the vertical blanking period begins.</p>
4:0	<p><b>Starting Row Scan Count.</b> This field provides all 5 bits of a 5-bit value that specifies the number of scan lines in a horizontal row of text. This value should be programmed to be equal to the number of scan lines in a horizontal row of text, minus 1.</p>

1



## 2.6.12 CR0A —Text Cursor Start Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=0Ah)  
 Default: 00UU UUUUb (U=Undefined)  
 Attributes: Read/Write



Bit De	scription
7:6	<b>Reserved.</b> Read as 0.
5	<p><b>Text Cursor Off.</b> This cursor is the text cursor that is part of the VGA standard, and should not be confused with the hardware cursor and popup which are intended to be used in extended graphics modes only. This text cursor exists only in text modes, and thus, this register is entirely ignored in graphics modes.</p> <p>0 = Enables the text cursor.            1 = Disables the text cursor.</p>
4:0	<p><b>Text Cursor Start.</b> This field specifies which horizontal line of pixels in a character box is to be used to display the first horizontal line of the cursor in text mode. The horizontal lines of pixels in a character box are numbered from top to bottom, with the top-most line being number 0. The value specified by these 5 bits should be the number of the first horizontal line of pixels on which the cursor is to be shown.</p>





## 2.6.15 CR0D —Start Address Low Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=0Dh)  
 Default: Undefined  
 Attributes: Read/Write

Bit De	scription
7:0	<p><b>Start Address Bits [7:0].</b> This register provides either bits 7 through 0 of a 16 bit value that specifies the memory address offset from the beginning of the frame buffer at which the data to be shown in the active display area begins. (default is 0)</p> <p>In standard VGA modes the start address is specified with a 16-bit value. The eight bits of the Start Address High Register (CR0C) provide the eight most significant bits of this value, while the eight bits of this register provide the eight least significant bits.</p>

## 2.6.16 CR0E —Text Cursor Location High Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=0Eh)  
 Default: Undefined  
 Attributes: Read/Write

Bit De	scription
7:0	<p><b>Text Cursor Location Bits [15:8].</b> This field provides the 8 most significant bits of a 16-bit value that specifies the address offset from the beginning of the frame buffer at which the text cursor is located. Bit 7:0 of the Text Cursor Location Low Register (CR0F) provide the 8 least significant bits.</p>

## 2.6.17 CR0F —Text Cursor Location Low Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=0Fh)  
 Default: Undefined  
 Attributes: Read/Write

Bit De	scription
7:0	<p><b>Text Cursor Location Bits [7:0].</b> This field provides the 8 least significant bits of a 16-bit value that specifies the address offset from the beginning of the frame buffer at which the text cursor is located. Bits 7:0 of the Text Cursor Location High Register (CR0D) provide the 8 most significant bits.</p>



## 2.6.18 CR10 —Vertical Sync Start Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=10h)

Default: Undefined

Attributes: Read/Write

Bit De	scription
7:0	<p><b>Vertical Sync Start Bits [7:0].</b> This register provides the 8 least significant bits of a 10-bit that specifies the beginning of the vertical sync pulse relative to the beginning of the active display area of a screen. In standard VGA modes, this value is described in 10 bits with bits [7,2] of the Overflow Register (CR07) supplying the 2 most significant bits.</p> <p>This 10-bit value should equal the vertical sync start in terms of the number of scan lines from the beginning of the active display area to the beginning of the vertical sync pulse. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which the vertical sync pulse begins.</p>

## 2.6.19 CR11 —Vertical Sync End Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=11h)

Default: 0U00 UUUUb (U=Undefined)

Attributes: Read/Write

7	6	5	4	3	0
Protect Regs 0:7	Reserved	Vert Int Enable	Vert Int Clear	Vertical Sync End	

Bit De	scription
7	<p><b>Protect Registers [0:7].</b> Note that the ability to write to Bit 4 of the Overflow Register (CR07) is not affected by this bit (i.e., bit 4 of the Overflow Register is always writeable).</p> <p>0 = Enable writes to registers CR[00:07]. (default) 1 = Disable writes to registers CR[00:07].</p>
6	<p><b>Reserved.</b> In the VGA standard, this bit was used to switch between 3 and 5 frame buffer refresh cycles during the time required to draw each horizontal line.</p>
5	<p><b>Vertical Interrupt Enable.</b> This bit is reserved for compatibility only. While this bit may be written or read, it's value will have no effect. Note that the VGA does not provide an interrupt signal which would be connected to an input of the system's interrupt controller. Bit 7 of Input Status Register 0 (ST00) originally indicated the status of the vertical retrace interrupt.</p> <p>0 = Enable the generation of an interrupt at the beginning of each vertical retrace period. 1 = Disable the generation of an interrupt at the beginning of each vertical retrace period.</p>
4	<p><b>Vertical Interrupt Clear.</b> This is reserved for compatibility only. Note that the VGA does not provide an interrupt signal which would be connected to an input of the system's interrupt controller.</p> <p>0 = Setting this bit to 0 clears a pending vertical retrace interrupt. This bit must be set back to 1 to enable the generation of another vertical retrace interrupt.</p>



Bit De	scription
3:0	<b>Vertical Sync End.</b> This 4-bit field provides a 4-bit value that specifies the end of the vertical sync pulse relative to its beginning. This 4-bit value should be set to the least significant 4 bits of the result of adding the length of the vertical sync pulse in terms of the number of scan lines that occur within the length of the vertical sync pulse to the value that specifies the beginning of the vertical sync pulse (see the description of the Vertical Sync Start Register for more details).

## 2.6.20 CR12 —Vertical Display Enable End Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=12h)  
 Default: Undefined  
 Attributes: Read/Write

Bit De	scription
7:0	<b>Vertical Display Enable End Bits [7:0].</b> This register provides the 8 least significant bits of a 10-bit value that specifies the number of the last scan line within the active display area. In standard VGA modes, this value is described in 10 bits with bits [6,1] of the Overflow Register (CR07) supplying the 2 most significant bits. This 10-bit value should be programmed to be equal to the number of the last scan line within in the active display area. Since the active display area always starts on the 0th scan line, this number should be equal to the total number of scan lines within the active display area, minus 1.

## 2.6.21 CR13 —Offset Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=13h)  
 Default: Undefined  
 Attributes: Read/Write

Bit De	scription
7:0	<b>Offset Bits [7:0].</b> This register provides either all 8 bits of an 8-bit value that specifies the number of words or DWords of frame buffer memory occupied by each horizontal row of characters. Whether this value is interpreted as the number of words or DWords is determined by the settings of the bits in the Clocking Mode Register (SR01).  In standard VGA modes, the offset is described with an 8-bit value, all the bits of which are provided by this register. This 8-bit value should be programmed to be equal to either the number of words or DWords (depending on the setting of the bits in the Clocking Mode Register, SR01) of frame buffer memory that is occupied by each horizontal row of characters.



## 2.6.22 CR14 —Underline Location Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=14h)  
 Default: 0UUU UUUUb (U=Undefined)  
 Attributes: Read/Write

7	6	5	4	0
Reserved (0)	Dword Mode	Count By 4	Underline Location	

Bit De	scription															
7	<b>Reserved.</b> Read as 0.															
6	<p><b>DWord Mode.</b></p> <p>0 = Frame buffer addresses are interpreted by the frame buffer address decoder as being either byte addresses or word addresses, depending on the setting of bit 6 of the CRT Mode Control Register (CR17).</p> <p>1 = Frame buffer addresses are interpreted by the frame buffer address decoder as being DWord addresses, regardless of the setting of bit 6 of the CRT Mode Control Register (CR17).</p> <p>Note that this bit is used in conjunction with bits 6 and 5 of the CRT Mode Control Register (CR17) to select how frame buffer addresses from the CPU are interpreted by the frame buffer address decoder as shown below:</p> <table border="1"> <thead> <tr> <th>CR14[6]</th> <th>CR17[ 6]</th> <th>Addressing Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Word Mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>Byte Mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>DWord Mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>DWord Mode</td> </tr> </tbody> </table>	CR14[6]	CR17[ 6]	Addressing Mode	0	0	Word Mode	0	1	Byte Mode	1	0	DWord Mode	1	1	DWord Mode
CR14[6]	CR17[ 6]	Addressing Mode														
0	0	Word Mode														
0	1	Byte Mode														
1	0	DWord Mode														
1	1	DWord Mode														
5	<p><b>Count By 4.</b></p> <p>0 = The memory address counter is incremented either every character clock or every other character clock, depending upon the setting of bit 3 of the CRT Mode Control Register.</p> <p>1 = The memory address counter is incremented either every 4 character clocks or every 2 character clocks, depending upon the setting of bit 3 of the CRT Mode Control Register. . This is used in mode x13 to allow for using all four planes.</p> <p>Note that this bit is used in conjunction with bit 3 of the CRT Mode Control Register (CR17) to select the number of character clocks are required to cause the memory address counter to be incremented as shown, below:</p> <table border="1"> <thead> <tr> <th>CR14[5]</th> <th>CR17[3]</th> <th>Address Incrementing Interval</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>every character clock</td> </tr> <tr> <td>0</td> <td>1</td> <td>every 2 character clocks</td> </tr> <tr> <td>1</td> <td>0</td> <td>every 4 character clocks</td> </tr> <tr> <td>1</td> <td>1</td> <td>every 2 character clocks</td> </tr> </tbody> </table>	CR14[5]	CR17[3]	Address Incrementing Interval	0	0	every character clock	0	1	every 2 character clocks	1	0	every 4 character clocks	1	1	every 2 character clocks
CR14[5]	CR17[3]	Address Incrementing Interval														
0	0	every character clock														
0	1	every 2 character clocks														
1	0	every 4 character clocks														
1	1	every 2 character clocks														



Bit De	scription
4:0	<b>Underline Location.</b> This field specifies which horizontal line of pixels in a character box is to be used to display a character underline in text mode. The horizontal lines of pixels in a character box are numbered from top to bottom, with the top-most line being number 0. The value specified by these 5 bits should be the number of the horizontal line on which the character underline mark is to be shown.

### 2.6.23 CR15—Vertical Blanking Start Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=15h)  
 Default: Undefined  
 Attributes: Read/Write

Bit De	scription
7:0	<b>Vertical Blanking Start Bits [7:0].</b> This register provides the 8 least significant bits of a 10-bit value that specifies the beginning of the vertical blanking period relative to the beginning of the active display area of the screen. In standard VGA modes, the vertical blanking start is specified with a 10-bit value. The most and second-most significant bits of this value are supplied by bit 5 of the Maximum Scan Line Register (CR09) and bit 3 of the Overflow Register (CR07), respectively. This 10-bit value should be programmed to be equal the number of scan lines from the beginning of the active display area to the beginning of the vertical blanking period. Since the active display area always starts on the 0th scan line, this number should be equal to the number of the scan line on which vertical blanking begins.

### 2.6.24 CR16—Vertical Blanking End Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=16h)  
 Default: Undefined  
 Attributes: Read/Write

This register provides a 8-bit value that specifies the end of the vertical blanking period relative to its beginning.

Bit De	scription
7:0	<b>Vertical Blanking End Bits [7:0].</b> This 8-bit value should be set equal to the least significant 8 bits of the result of adding the length of the vertical blanking period in terms of the number of scan lines that occur within the length of the vertical blanking period to the value that specifies the beginning of the vertical blanking period (see the description of the Vertical Blanking Start Register for details).



## 2.6.25 CR17 —CRT Mode Control

I/O (and Memory Offset) Address: 3B5h/3D5h (index=17h)  
 Default: 0UU0 UUUUb (U=Undefined)  
 Attributes: Read/Write

7	6	5	4	3	2	1	0
CRT Ctrl Reset	Word or Byte Mode	Address Wrap	Reserved (0)	Count By 2	Horizontal Retrace Select	Select Row Scan Cntr	Compat Mode Support

Bit De	scription															
7	<p><b>CRT Controller Reset.</b> This bit has no effect except in native VGA modes (non-centered).</p> <p>0 = Forces horizontal and vertical sync signals to be inactive. No other registers or outputs are affected.</p> <p>1 = Permits normal operation.</p>															
6	<p><b>Word Mode or Byte Mode.</b></p> <p>0 = The memory address counter's output bits are shifted by 1 bit position before being passed on to the frame buffer address decoder such that they are made into word-aligned addresses when bit 6 of the Underline Location Register (CR17) is set to 0.</p> <p>1 = The memory address counter's output bits remain unshifted before being passed on to the frame buffer address decoder such that they remain byte-aligned addresses when bit 6 of the Underline Location Register (CR17) is set to 0.</p> <p>Note that this bit is used in conjunction with bits 6 and 5 of the CRT Mode Control Register (CR17) to control how frame buffer addresses from the memory address counter are interpreted by the frame buffer address decoder as shown below:</p> <table border="1"> <thead> <tr> <th>CR14[6]</th> <th>CR17[6]</th> <th>Addressing Mode</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>Word Mode—Addresses from the memory address counter are shifted once to become word-aligned</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Byte Mode—Addresses from the memory address counter are not shifted</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>DWord Mode—Addresses from the memory address counter are shifted twice to become DWord-aligned</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>DWord Mode—Addresses from the memory address counter are shifted twice to become DWord-aligned</td> </tr> </tbody> </table>	CR14[6]	CR17[6]	Addressing Mode	0	0	Word Mode—Addresses from the memory address counter are shifted once to become word-aligned	0	1	Byte Mode—Addresses from the memory address counter are not shifted	1	0	DWord Mode—Addresses from the memory address counter are shifted twice to become DWord-aligned	1	1	DWord Mode—Addresses from the memory address counter are shifted twice to become DWord-aligned
CR14[6]	CR17[6]	Addressing Mode														
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1	0	DWord Mode—Addresses from the memory address counter are shifted twice to become DWord-aligned														
1	1	DWord Mode—Addresses from the memory address counter are shifted twice to become DWord-aligned														
5	<p><b>Address Wrap.</b> Note that this bit is only effective when word mode is made active by setting bit 6 in both the Underline Location Register and this register to 0.</p> <p>0 = Wrap frame buffer address at 16 KB. This is used in CGA-compatible modes.</p> <p>1 = No wrapping of frame buffer addresses.</p>															
4	<p><b>Reserved.</b> Read as 0.</p>															



Bit Description	Description															
3	<p><b>Count By 2.</b> This bit is used in conjunction with bit 5 of the Underline Location Register (CR14) to select the number of character clocks are required to cause the memory address counter to be incremented.</p> <p>0 = The memory address counter is incremented either every character clock or every 4 character clocks, depending upon the setting of bit 5 of the Underline Location Register.</p> <p>1 = The memory address counter is incremented either every other clock.</p> <table border="1" data-bbox="347 506 935 701"> <thead> <tr> <th>CR14[5]</th> <th>CR17[3]</th> <th>Address Incrementing Interval</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>every character clock</td> </tr> <tr> <td>0</td> <td>1</td> <td>every 2 character clocks</td> </tr> <tr> <td>1</td> <td>0</td> <td>every 4 character clocks</td> </tr> <tr> <td>1</td> <td>1</td> <td>every 2 character clocks</td> </tr> </tbody> </table>	CR14[5]	CR17[3]	Address Incrementing Interval	0	0	every character clock	0	1	every 2 character clocks	1	0	every 4 character clocks	1	1	every 2 character clocks
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0	0	every character clock														
0	1	every 2 character clocks														
1	0	every 4 character clocks														
1	1	every 2 character clocks														
2	<p><b>Horizontal Retrace Select.</b> This bit provides a way of effectively doubling the vertical resolution by allowing the vertical timing counter to be clocked by the horizontal retrace clock divided by 2 (usually, it would be undivided).</p> <p>0 = The vertical timing counter is clocked by the horizontal retrace clock.</p> <p>1 = The vertical timing counter is clocked by the horizontal retrace clock divided by 2.</p>															
1	<p><b>Select Row Scan Counter.</b></p> <p>0 = A substitution takes place, where bit 14 of the 16-bit memory address generated of the memory address counter (after the stage at which these 16 bits may have already been shifted to accommodate word or DWord addressing) is replaced with bit 1 of the row scan counter at a stage just before this address is presented to the frame buffer address decoder.</p> <p>1 = No substitution takes place. See following tables.</p>															
0	<p><b>Compatibility Mode Support.</b></p> <p>0 = A substitution takes place, where bit 13 of the 16-bit memory address generated of the memory address counter (after the stage at which these 16 bits may have already been shifted to accommodate word or DWord addressing) is replaced with bit 0 of the row scan counter at a stage just before this address is presented to the frame buffer address decoder.</p> <p>1 = No substitution takes place. See following tables.</p>															

The following tables show the possible ways in which the address bits from the memory address counter can be shifted and/or reorganized before being presented to the frame buffer address decoder. First, the address bits generated by the memory address counter are reorganized, if need be, to accommodate byte, word or DWord modes. The resulting reorganized outputs (MAOut15-MAOut0) from the memory address counter may also be further manipulated with the substitution of bits from the row scan counter (RSOut1 and RSOut0) before finally being presented to the input bits of the frame buffer address decoder (FBIn15-FBIn0).



**Table 2-2. Memory Address Counter Address Bits [15:0]**

By	te Mode CR14 bit 6=0 CR17 bit 6=1 CR17 bit 5=X	Word Mode CR14 bit 6=0 CR17 bit 6=0 CR17 bit 5=1	Word Mode CR14 bit 6=0 CR17 bit 6=0 CR17 bit 5=0	DWord Mode CR14 bit 6=1 CR17 bit 6=X CR17 bit 5=X
MAOut0	0	15	13	12
MAOut1	1	0	0	13
MAOut2	2	1	1	0
MAOut3	3	2	2	1
MAOut4	4	3	3	2
MAOut5	5	4	4	3
MAOut6	6	5	5	4
MAOut7	7	6	6	5
MAOut8	8	7	7	6
MAOut9	9	8	8	7
MAOut10	10	9	9	8
MAOut11	11	10	10	9
MAOut12	12	11	11	10
MAOut13	13	12	12	11
MAOut14	14	13	13	12
MAOut15	15	14	14	13

X = Don't Care

**Table 2-3. Frame Buffer Address Decoder**

	CR17 bit 1=1	CR17 bit 1=1	CR17 bit 1=0	CR17 bit 1=0
	CR17 bit 0=1	CR17 bit 0=0	CR17 bit 0=1	CR17 bit 0=0
FBIn0	MAOut0	MAOut0	MAOut0	MAOut0
FBIn1	MAOut1	MAOut1	MAOut1	MAOut1
FBIn2	MAOut2	MAOut2	MAOut2	MAOut2
FBIn3	MAOut3	MAOut3	MAOut3	MAOut3
FBIn4	MAOut4	MAOut4	MAOut4	MAOut4
FBIn5	MAOut5	MAOut5	MAOut5	MAOut5
FBIn6	MAOut6	MAOut6	MAOut6	MAOut6
FBIn7	MAOut7	MAOut7	MAOut7	MAOut7
FBIn8	MAOut8	MAOut8	MAOut8	MAOut8
FBIn9	MAOut9	MAOut9	MAOut9	MAOut9
FBIn10	MAOut10	MAOut10	MAOut10	MAOut10
FBIn11	MAOut11	MAOut11	MAOut11	MAOut11
FBIn12	MAOut12	MAOut12	MAOut12	MAOut12
FBIn13	MAOut13	MAOut13	RSOut0	RSOut0
FBIn14	MAOut14	RSOut1	MAOut14	RSOut1
FBIn15	MAOut15	MAOut15	MAOut15	MAOut15



## 2.6.26 CR18 —Line Compare Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=18h)  
 Default: Undefined  
 Attributes: Read/Write

Bit De	scription
7:0	<p><b>Line Compare Bits [7:0].</b> This register provides the 8 least significant bits of a 10-bit value that specifies the scan line at which the memory address counter restarts at the value of 0. Bit 6 of the Maximum Scan Line Register (CR09) supplies the most significant bit, and bit 4 of the Overflow Register (CR07) supplies the second most significant bit.</p> <p>Normally, this 10-bit value is set to specify a scan line after the last scan line of the active display area. When this 10-bit value is set to specify a scan line within the active display area, it causes that scan line and all subsequent scan lines in the active display area to display video data starting at the very first byte of the frame buffer. The result is what appears to be a screen split into a top and bottom part, with the image in the top part being repeated in the bottom part. (This register is only used in split screening modes, and this is not a problem because split screening is not actually used for extended modes. As a result, there is no benefit to extending the existing overflow bits for higher resolutions. )</p> <p>When used in cooperation with the Start Address High Register (CR0C) and the Start Address Low Register (CR0D), it is possible to create a split display, as described earlier, but with the top and bottom parts displaying different data. The top part will display whatever data exists in the frame buffer starting at the address specified in the two aforementioned start address registers, while the bottom part will display whatever data exists in the frame buffer starting at the first byte of the frame buffer.</p>

## 2.6.27 CR22 —Memory Read Latch Data Register

I/O (and Memory Offset) Address: 3B5h/3D5h (index=22h)  
 Default: 00h  
 Attributes: Read Only

Bit De	scription
7:0	<p><b>Memory Read Latch Data.</b> This field provides the value currently stored in 1 of the four memory read latches. Bits 1 and 0 of the Read Map Select Register (GR04) select which of the four memory read latches may be read via this register.</p>